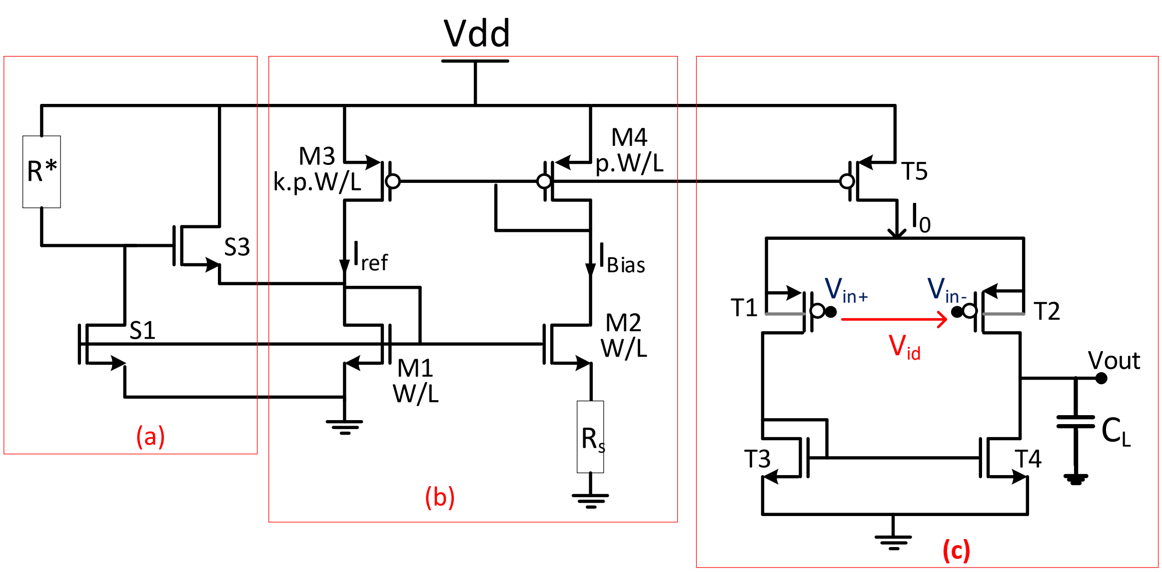
I/g_m Design Methodology

EKV Parameters for 1.2V Standard MOST of UMC 65nm technology

Transistor N	Transistor P	
$k_{P,n}$= 300 µA/V^2 n= 1.2 V_{T0}= 0.4 V $U_{a,N}$= 10 V/µm C_{ox}= 13 fF/µm^2 $C_{gs,ov} = C_{gd,ov} = C_{ov}$ =0.2 fF/µm	$k_{P,p}$= 110 µA/V^2 n= 1.3 V_{T0}= 0.4 V $U_{a,P}$= 10 V/µm C_{ox}= 13 fF/µm^2 C_{ov} =0.2 fF/µm	**V_{DD} = 1.2V** **$V_{GND} = V_{SS}$ =0V**

Given the following OTA and its bias circuit:



OTA with PMOS differential pair and its Bias circuits

1. Explain the role of the circuits a, b, c

- Explain the operation of (a).

The circuit (a) is a start-up circuit that will enable to avoid the degenerated state $I_{ref} = 0$ of the β-multiplier (b). In fact, when I_{ref} is null, $V_{GS,S3}$ equals V_{dd} and a significant current is injected by S3 into the drain of M1. This will trigger the positive feedback and set I_{bias} to its desired study-state value defined by R_s. At the same time $V_{GS,S3}$ decreases and should go blow V_{T0} at the study state to cancel the impact of the start-up circuit on the β-multiplier operation.

- Explain the operation of (b) and size all its transistors and R_s to meet the following specifications: **I_{Bias}** = 10 µA, I_F of M2, M3, M4 is 10 and k = 4.

The circuit (b) is a Beta-multiplier.

The pMOS mirror impose: $I_{Bias} = \frac{I_{ref}}{k} \rightarrow \frac{\beta_2}{2}\left(V_{g2} - R_s I_{Bias} - V_T\right)^2 = \frac{\beta_1}{2k}\left(V_{g1} - V_T\right)^2 = I_{Bias}$

$$\rightarrow \left(V_{g1,2} - V_T\right) = \sqrt{\frac{2kI_{Bias}}{\beta_1}} \rightarrow I_{Bias} = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2kI_{Bias}}{\beta_1}} - R_s I_{Bias}\right)^2$$

And thus if ($I_{Bias} \neq 0$) we have:

$$\mathbf{I_{Bias}} = \frac{\mathbf{2}}{\boldsymbol{\beta_1 R_s^2}}\left(\sqrt{\mathbf{k}} - \mathbf{1}\right)^2$$

Since we know I_F of M2 we can calculate its (W/L)

$$M2 \rightarrow \left(\frac{W}{L}\right)_{1,2} = \frac{\boldsymbol{I_{Bias}}}{\mathbf{2} \times \boldsymbol{n_n} \times \boldsymbol{k_{pn}} \times \boldsymbol{I_{F2}} \times \boldsymbol{u_T^2}} = \frac{10.10^{-6}}{2 \times 1.2 \times 300\ 10^{-6} \times 10 \times (26.10^{-3})^2} = 2$$

$$R_s = \sqrt{\frac{2}{\boldsymbol{k_{pn}}\left(\frac{W}{L}\right)_1 \boldsymbol{I_{Bias}}}\left(\sqrt{\mathrm{k}} - 1\right)^2} = \sqrt{\frac{2}{300\ 10^{-6}\ 2\ 10\ 10^{-6}}} = 18\ k\Omega$$

$$M4 \rightarrow \left(\frac{W}{L}\right)_4 = \frac{\boldsymbol{I_{Bias}}}{\mathbf{2} \times \boldsymbol{n_p} \times \boldsymbol{k_{pp}} \times \boldsymbol{I_{F4}} \times \boldsymbol{u_T^2}} = \frac{10.10^{-6}}{2 \times 1{,}3 \times 110\ 10^{-6} \times 10\ \times (26.10^{-3})^2} = 5$$

$$M3 \rightarrow \left(\frac{W}{L}\right)_3 = 4\left(\frac{W}{L}\right)_4 = 20$$

- If the all nMOS transistors of (a) and (b) have the same size, propose a value for R*.

At study-state the transistor S3 should be switched off to don't disturb the Beta-multiplier. For this, the following conditions have to be fulfilled at study-state:

$$V_{gs}(S_3) < V_T \rightarrow V_{DD} - R^* I_{ref} - V_{gs}(M_1) < V_T \rightarrow R^* > \frac{V_{DD} - V_{gs}(M_1) - V_T}{I_{ref}}$$

M1 in strong inversion → $V_{gs}(M_1) = \sqrt{\frac{2I_{ref}}{k_{pn}\left(\frac{W}{L}\right)_1}} + V_T = \sqrt{\frac{2.40.10^{-6}}{300.10^{-6}.2}} + 0{,}4 = 0.77\ V \rightarrow R^* > \frac{1.2-0.77-0.4}{40.10^{-6}} \rightarrow$

$R^* > 750\ \Omega$

2. Given the following specifications, size all the transistors of the OTA (b)

The circuit will be designed to meet the following specifications, which will be verified by simulation.

Parameter	Unit	
	Specification	
Open-loop Gain: $\mathbf{A_o}$	≈ 35 dB (56)	dB
GBW: $\mathbf{f_{GBW}}$	25	MHz
Slew rate: **SR**	20	V/µs
Load Capacitance: $\mathbf{C_L}$	1	pF
$\mathbf{I_{F,5}}$	10	

<u>SizingThe OTA will now be sized. Calculate the following parameters in the proposed order.</u>

	Parameter	Expression	Value	Unit	Guideline
Bias	I_0	$I_0 = S_r \cdot C_L$	20	µA	
	$\frac{W_5}{L_5}$	$\frac{I_{D5}}{2 \times n \times k_p \times I_f \times u_T^2}$	5	µm	$L_5 = 0.5\mu m$
Differential pair	g_{m2}	$f_{gbw} \times 2 \times \pi \times C_L$	157	µS	*GBW*
	$\frac{g_{m2}}{I_{d2}}$		15.7	V^{-1}	
	$I_{F1,2}$	$\left(\frac{1}{\left(n \times u_T \times \frac{g_{m1,2}}{I_{D1,2}}\right)} - \frac{1}{2}\right)^2 - \frac{1}{4}$	1.66	-	$I_F = I_c$ *is the inversion factor*
		Conclusion about the operation of m1, m2	MI		*Strong or weak inversion*
	$\frac{W_{1,2}}{L_{1,2}}$	$\frac{I_{D1,2}}{2 \times n \times k_p \times I_f \times u_T^2}$	31	-	
	R_{out}	$\frac{A_0}{g_{m1,2}}$	357	kΩ	A_o
	$L_{1,2}$	$= R_{out} I_D \left(U_{a,n}^{-1} + U_{a,p}^{-1}\right)$	0.7	µm	R_{out}, $L_4 = L_2$
	$W_{1,2}$		22	µm	
	$\frac{W_4}{L_4}$	$\frac{I_{D4}}{2 \times n \times k_p \times I_f \times u_T^2}$	2	-	$I_F = 10$
	L_4		0.7	µm	$L_2 = L_4$
	W_4		1.4	µm	
	g_{m4}	$\frac{g_m}{I_D} = \frac{1}{nU_T} \cdot \frac{2}{1 + \sqrt{4I_F + 1}}$	86.6	µS	$\frac{g_m}{I_D} = 8.7$

4. Determine analytically

- **the common mode input range CMIR⁺/ CMIR⁻**
- **the output swing**
- **the poles (dominant and non dominant)**
- **the phase margin PM**
- **CMRR**

	Analytical expression	Numerical value
A [dB]	$A_0 = g_{m2}.R_{out}$	56 (35dB)
f_{dom} [Hz]	$\frac{1}{2\pi R_{out} C_L}$	446k
f_{nondom} [Hz] (neglect junction cap C_{SB}, C_{DB})	$\frac{g_{m4}}{2\pi(C_{gd} + C_{gs3} + C_{gs4} + g_{m4} R_{out} C_{gd})}$ $\frac{g_{m4}}{2\pi\left(C_{ov}W_2 + 2.\left(\frac{C_{ox}W_4L_4.2}{3} + C_{ov}W_4\right) + g_{m4}R_{out}C_{ov}W_4\right)}$ $\frac{86.6\ 10^{-6}}{2\pi(4.4\ 10^{-1} + 2 \times 8.77\ 10^{-15} + 8.7\ 10^{-15})}$	450 M >> GBW
PM [°]	$180° - \arctan\left(\frac{f_{GBW}}{f_{dom}}\right) - \arctan\left(\frac{f_{GBW}}{f_{non-dom}}\right)$	90°
CMIR⁺ [V]	$V_{DD} - V_{SD,sat5} - V_{sg1}$	0.6
CMIR⁻ [V]	$V_{s,min} - V_{sg1} = V_{SD,sat1} + V_{sg3} - V_{sg1} \approx 4U_T + 0.6 - V_{Tn}$	0.3
V_{OUTmax} [V]	$V_{s2} - V_{SD,sat2} = V_{in-} + V_{sg2} - V_{SD,sat21} \approx 0.5 + V_{Tp} - 4U_T$ (if $V_{in-} = 0.5$ V)	0.8
V_{OUTmin} [V]	$V_{D,sat4}$	0.2
ΔV_{OUT} [V]	$V_{out,max} - V_{out,min}$	0.4